Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-17 (canceled)

18. (currently amended) An isolation structure, comprising:

a first area and a second area;

a plurality of shallow isolation trenches in the first area; and

a plurality of deep isolation trenches in the second area, the deep isolation trenches and the shallow isolation trenches being ~~perfectly~~ self-aligned.

19. (original) The isolation structure of claim 18, wherein the plurality of shallow trenches are between approximately 1000 Å to 2000 Å in depth.

20. (original) The isolation structure of claim 18, wherein the plurality of deep isolation trenches are between approximately 3000 Å to 6000 Å in depth.

21. (new) The isolation structure of claim 18, wherein the first area includes memory devices.

22. (new) The isolation structure of claim 21, wherein the memory devices comprise flash memory devices.

23. (new) The isolation structure of claim 18, wherein the second area includes logic devices.

24. (new) The isolation structure of claim 18, wherein the widths of the shallow isolation trenches are less than the widths of the deep isolation trenches.

25. (new) The isolation structure of claim 18, further comprising:

a thin thermal oxide in the shallow isolation trenches.

26. (new) The isolation structure of claim 18, further comprising:

a trench fill material in the shallow isolation trenches.

27. (new) The isolation structure of claim 18, further comprising:

a first active region in the first area; and

a second active region in the second area.

28. (new) The isolation structure of claim 27, further comprising:

a mask layer on the first active region.

29. (new) The isolation structure of claim 28, wherein the mask layer comprises a pad oxide layer and a nitride layer.

30. (new) The isolation structure of claim 29, wherein the mask layer comprises an antireflective coating.

31. (new) The isolation structure of claim 18, further comprising:

a photoresist layer covering the first area, wherein the photoresist layer leaves the second area exposed.

32. (new) An apparatus comprising:

a substrate having self-aligned deep and shallow isolation trenches.

33. (new) The apparatus of claim 32, wherein the substrate comprises monocrystalline silicon.

34. (new) The apparatus of claim 32, wherein the shortest distance between a shallow isolation trench and an adjacent deep isolation trench is greater than the allowed error of a non-critical photolithography mask.

35. (new) The apparatus of claim 34, wherein the allowed error is in the range of about 150 to 300 nm.

36. (new) The apparatus of claim 32, wherein the deep isolation trenches isolate active regions including high voltage logic devices.

37. (new) The apparatus of claim 32, wherein the shallow isolation trenches isolate active regions including memory devices.

38. (new) The apparatus of claim 32, wherein the shallow isolation trenches isolate flash memory cell columns.

39. (new) An apparatus comprising:

a substrate including a first area and a second area;

a plurality of shallow isolation trenches in the first area;

a plurality of deep isolation trenches in the second area, the deep isolation trenches and the shallow isolation trenches being self-aligned using a single photolithography step;

a plurality of memory devices in the first area; and

a plurality of logic devices in the second area.

40. (new) The apparatus of claim 39, wherein the memory devices comprise flash memory devices.

41. (new) The apparatus of claim 40, wherein the logic devices comprise transistors to control the flash memory devices.